

Users Guide for the Dual Phase Detector Module Prototype

For Booster Acceleration and MI Phase Lock Control

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I. Introduction

The Dual Phase Detector Module has many features that make it flexible and hence potentially complicated for the user. Implemented within the FPGA are registers for setting gain, offsets and other parameters. Non-volatile memory is used on the module to retain settings once they are made. The current prototype version does not have a computer interface and does not include an onboard processor. This was an experiment to try to put bounds on the complexity of the final product (i.e. no software to keep track of). The features and methods developed on this version of the module may very well migrate to a more complex system in the future.

The goal for this module is to be able to provide the phase error feedback and control used to perform the Booster acceleration phase lock and the Main Injector phase lock functions. In doing this, this module could eventually replace the following LLRF NIM modules:

1. The Timing Generator, 0331.00-ED-180859
2. The 32 Countdown Module, 0331.00-EC-180846
3. The High Stability EMI Protected Phase Detector
4. The Program Generator, 0331.00-ED-180850
5. The Parabola Zero Box, 0331.00-EC-180858
6. The Fast Phase Detector, 0331.00-ED-180843
7. The Mode Controller, 0331.00-ED-180845

There are currently two Dual Phase Detector Modules assembled and being carried along through the firmware development and testing. Opportunities for testing these modules with the rest of the LLRF system and with Booster beam are rare, but some progress has been made. A second version of the module has been designed and the printed circuit laid out. Further testing will be done with the current version before finalizing and producing the next version.

II. Programmer Monitor Unit

In order to program the various registers on the module a simple hardware based module was built to interface with the boards. This programmer/monitor unit is also a NIM module and connects to the Phase Detector Module through two ribbon cable connections. The registers are selected using two 4 Bit Hex switches, S1 and S2. The register values are adjusted using a dial encoder. The values of the registers are monitored using seven-segment Hex displays. There are two additional switches that select the gain of the dial encoders so that the user can scale the response to an encoder step, effectively selecting the Hex digit that is incremented or decremented.

This document provides a schematic of the user interface, the Hex addresses of the programmable registers, other diagnostic capabilities and interesting details.

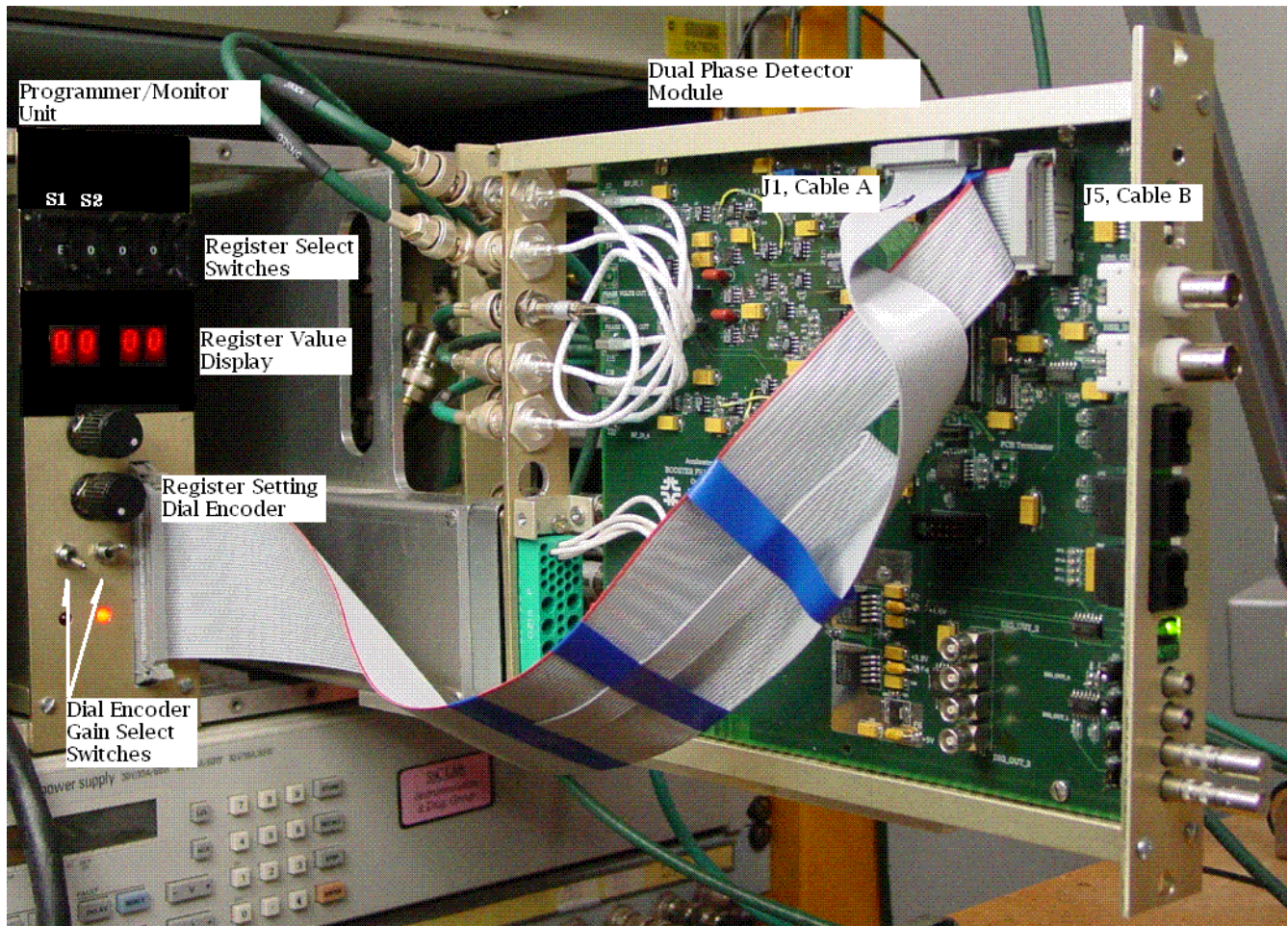


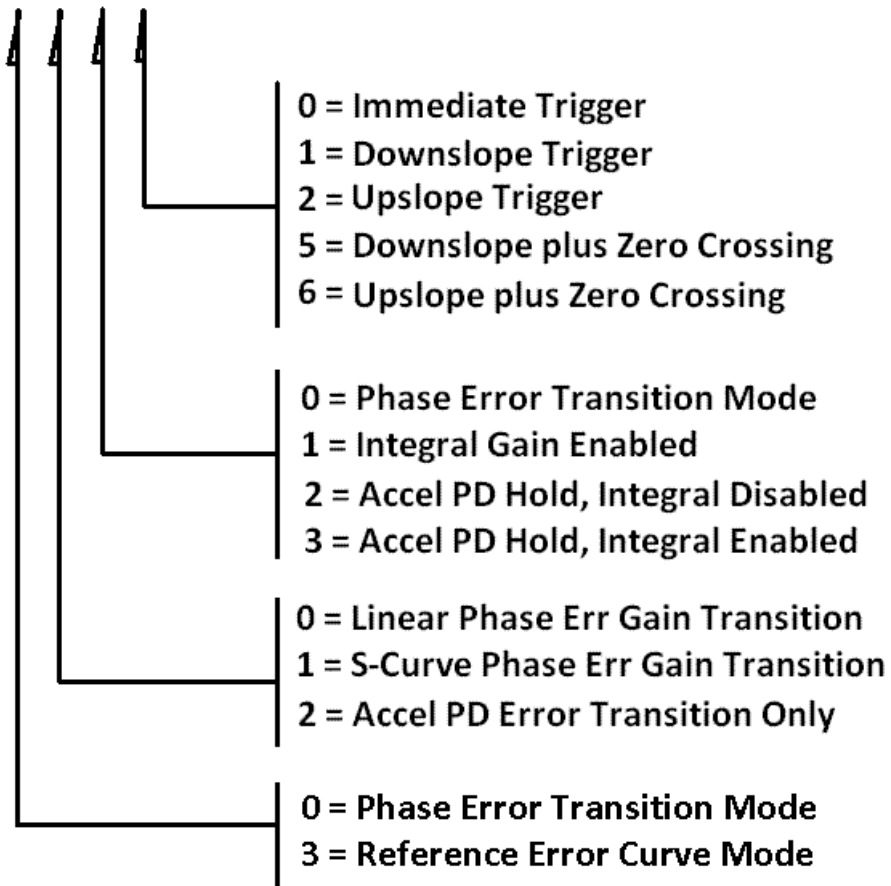
Table II.1 Abbreviated Memory Map for Setting Gains and Offsets

Register Name	Address (Hex Switch Setting)	Data Format	Description										
Channel A Gain (Acceleration Phase Detector Gain)	E0xx	12 Bit Offset Binary	This is the gain of the upper channel A. The value is a 12 bit offset binary number where 0x0000 is a gain of –1.0 0x0800 is a gain of 0.0 0x0FFF is a gain of +1.0										
Channel A Offset (Acceleration Phase Detector Offset)	E1xx	12 Bit Offset Binary	This is an offset of the upper channel A. The value is a 12 bit offset binary number where 0x0000 is an offset of approx. –2.5 V 0x0800 is an offset of 0.0 V 0x0FFF is an offset of approx. +2.5 V										
Channel B Gain (MI Phase Detector Gain)	E2xx	-- Offset Binary	<table><tr><td>This is the gain of the lower channel B.</td><td></td></tr><tr><td>Direct Feedback Mode 12 Bit Offset Binary</td><td>Reference Error Curve Mode 14 Bit Offset Binary</td></tr><tr><td>0x0000 is a gain of –1.0</td><td>0x0000 is a gain of –1.0</td></tr><tr><td>0x0800 is a gain of 0.0</td><td>0x2000 is a gain of 0.0</td></tr><tr><td>0x0FFF is a gain of +1.0</td><td>0x3FFF is a gain of +1.0</td></tr></table>	This is the gain of the lower channel B.		Direct Feedback Mode 12 Bit Offset Binary	Reference Error Curve Mode 14 Bit Offset Binary	0x0000 is a gain of –1.0	0x0000 is a gain of –1.0	0x0800 is a gain of 0.0	0x2000 is a gain of 0.0	0x0FFF is a gain of +1.0	0x3FFF is a gain of +1.0
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0x0FFF is a gain of +1.0	0x3FFF is a gain of +1.0												
Channel B Offset (MI Phase Detector Offset)	E3xx	12 Bit Offset Binary	This is an offset of the upper channel B. The value is a 12 bit offset binary number where 0x0000 is an offset of approx. –2.5 V 0x0800 is an offset of 0.0 V 0x0FFF is an offset of approx. +2.5 V										
Curve Memory Starting Address Offset	E4xx	8 Bit Unsigned	In the Reference Error Curve Mode for the MI phase lock, this value is the offset from the start of the reference curve memory. See the section describing this MI phase lock mode.										
MI Phase Lock Gain and Ref. Curve Time Scaling	E5xx	14 Bit Unsigned	Channel A and Channel B Gain Curve Time Scaling 0x100 => 800 us transition interval 0x080 => 400 us										

			0x040 => 200 us 0x020 => 100 us 0x000 => Immediate Transition
MI Phase Lock Integral Gain	E6xx	14 Bit Offset Binary	Integral gain setting used with each MI phase lock mode. The MI PD Error is accumulated from the start of MIPL and multiplied by this gain.
Mode Select	E7xx	16 Bit	Selects different options and modes of operation for transitioning from the Acceleration phase lock and executing the MI phase lock. See the Mode Select figure below.
Trigger Slope Threshold	E8xx	14 Bit Offset Binary	The value is a 14 bit offset binary number where 0x2000 is nominally 0.0V. This adjusts what is considered the zero crossing when using MI phase lock trigger modes.
NO_BEAM_OFFSET	E9xx	14 Bit Offset Binary	This offset nulling value is applied to the Acceleration Phase Detector output when there is No Beam. It ensures that there is not an offset applied to the Frequency Source when doing MI phase lock test without beam, and can also zero the phase detector output just before the acceleration cycle begins.
reserved	EAxx		
Phase Error Scaling	EBxx	14 Bit Offset Binary	Used with the Reference Error Curve Mode for the MI phase lock. See the section describing this MI phase lock mode.

Mode Select, E7xx

0 x 0 0 0 0

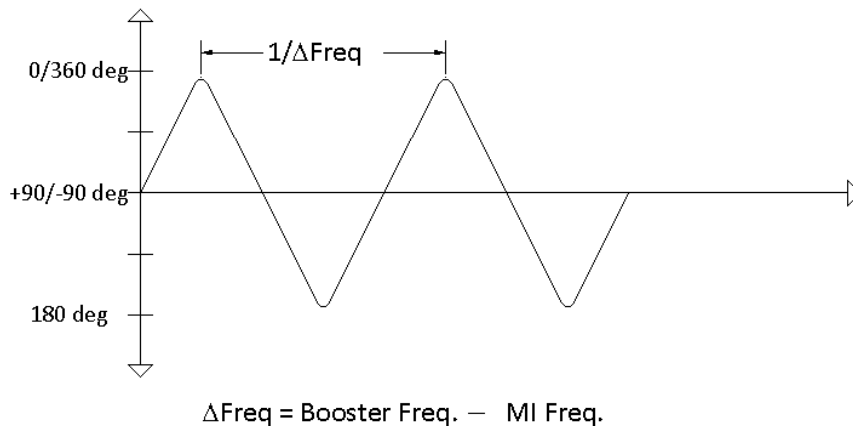


III. MI Phase Lock, Reference Error Curve Mode

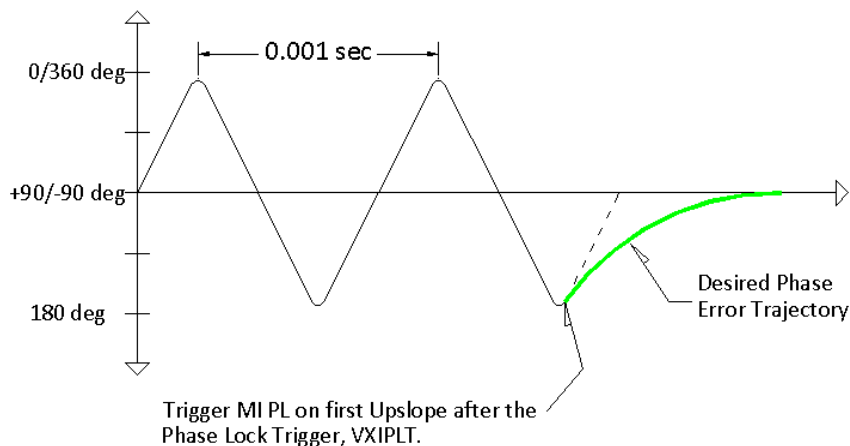
The MI Phase Lock Reference Error Curve Mode is a control method similar to the one originally used for phase locking the Booster LLRF frequency reference (and beam) to the MI frequency. The idea is to create a trajectory we wish the phase error to follow as it is being phase locked to the MI frequency. A block diagram of the method is given in Figure III.1.

The process proceeds as follows

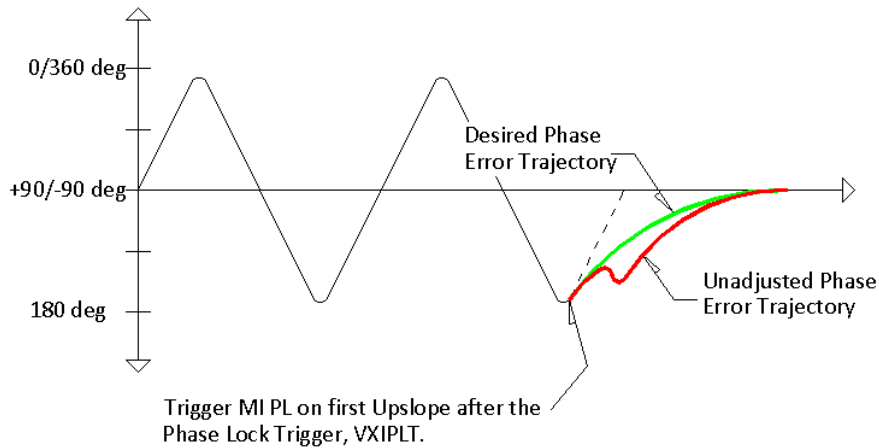
1. As the Booster LLRF frequency ramps towards the MI frequency the period of the triangle-wave output of the phase detector increases. The frequency source detects when it has reached a frequency out, 1000 Hz below the typical MI frequency of 52.813 MHz (52.812 MHz), and puts out a “begin phase lock” trigger.



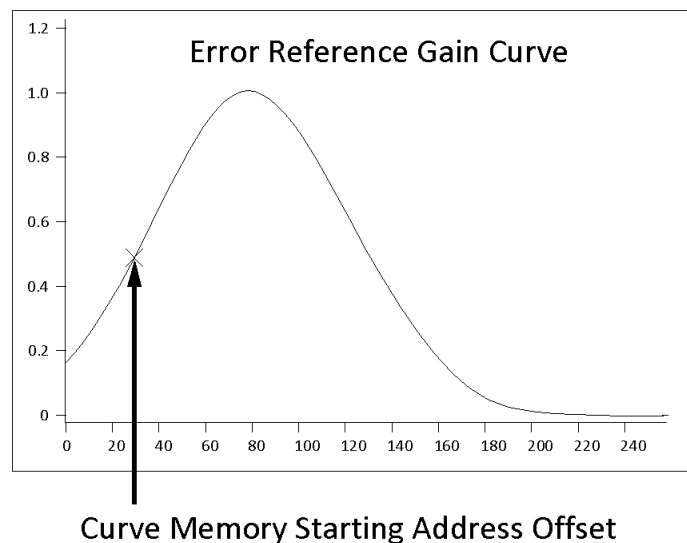
2. When the Dual Phase Detector Module sees this trigger the phase lock process begins on the next upslope of the phase detector output.
3. At the start of the phase lock process the phase detector phase error value is latched in one branch of the process and this starting value is subject to scaling by the Error Reference Gain Curve. The multiplication product, which changes from the original latched phase error to zero, according to the reference curve, becomes the desired phase error trajectory.
4. The changing phase error (not latched) is subtracted from the reference trajectory to produce the error signal used in our control loop to drive the actual phase error to follow this desired reference trajectory.



5. Adjustment is needed in this process to compensate for the fact that since the phase error we are trying to force to follow our desired trajectory, begins with its own trajectory with a non-zero time derivative. Latencies and time constants in our control loop will cause the phase error to initially “backup” to get on-track with our desired trajectory that begins at the phase error latched at the beginning of the process.



6. In order to present a trajectory that the phase error can smoothly follow we apply a gain curve that initially increases the latched phase error before driving the trajectory to zero. The first adjustment to smoothing the resulting phase error trajectory is to change where on the rising side of our reference gain curve that we begin.
7. The second adjustment matches the scale of the incoming phase error to the scale of the point where we start in our reference gain curve. That is our reference gain curve is normalized to be between 1 and 0. If we do not start at the peak of the gain curve we initially apply a gain less than 1 and we want to apply the same gain to the incoming phase error so when the phase error and trajectory are compared the difference is initially zero. The overall reduction in the feedback gain is compensated for by the control loop gain settings.



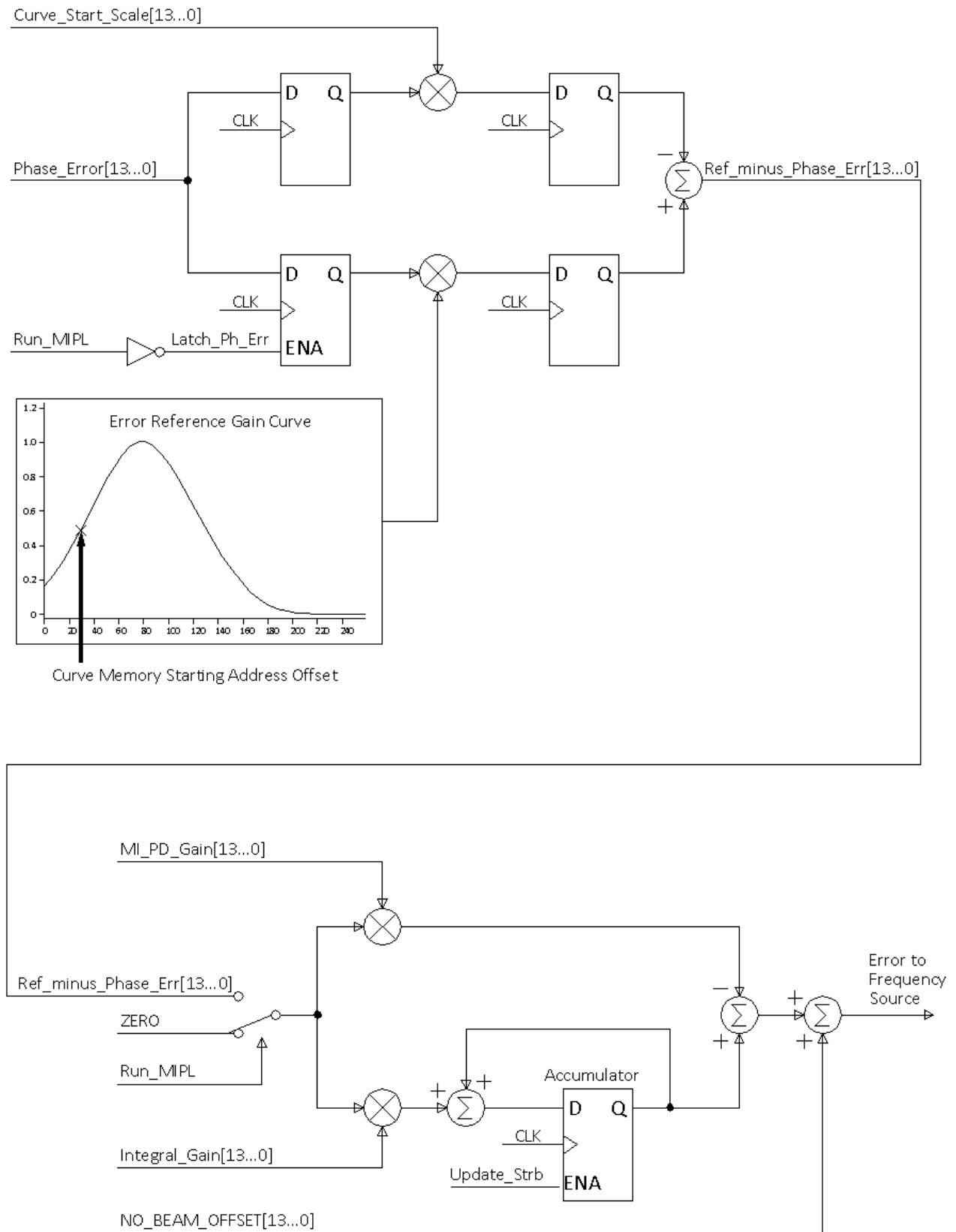


Figure III.1 Block diagram of the Reference Error Curve Mode processing.

This method of generating a reference trajectory and driving the LLRF frequency to follow this trajectory is sensitive, but not overly sensitive, to the frequency difference between the Booster RF and the MI RF at the start of the phase lock process. Nominally, we expect this difference to be 1000 Hz. Currently, we expect to still get good results between a frequency difference between 1500 and 500 Hz.

Notes:

1. Momentarily pressing the RESET button on the front of the phase detector module will cause an LED on the Programmer/Monitor Unit to blink and cause all of the programmable registers to be written into non-volatile memory.
2. Rotary hex switches SW2 and SW3, on the front of the Phase Detector Module, must both be set to 0 in order for the NIM interface module switches to work correctly.

